A New, Low-Cost, Sampled-Data, 10-Bit CMOS A/D Converter

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"IF IT'S NOT LOW COST, IT'S NOT CREATIVE"

Cost is the single most important factor in the success of any new product. The current emphasis on digital approaches to build electronic systems and the success of microprocessors have created new, high-volume markets for low cost A/D converters. Without this stimulation in the marketplace, converter products would not have been selected as monolithic components, due to the relatively low volume usage of the traditional products. The challenge today, therefore, is to find new design solutions which will reduce costs of A/Ds without sacrificing the performance specifications.

HOW MANY BITS ARE NEEDED?

The question of how many bits are needed in the A/D converter for a particular system is not always easy to answer. This is further complicated because of the distinction which must first be made between resolution and accuracy. For example, your digital bathroom scale may have graduations which indicate each pound over a range which extends from zero to 300 pounds maximum. This means you are capable of "resolving" one pound over this complete dynamic range or "span." The next question is, "What do I really weigh, say, on my doctor's scale?" You may find that his scale indicates you are actually three pounds heavier than your scale indicates: this is the accuracy problem.

A 10-bit A/D is capable of resolving 2^{10}, or 1024, minimum voltage levels over the range from 0 to V_{REF} volts. To put this into the physical world we live in, this degree of resolution is capable of differentiating each single sheet of paper, which is only 0.004 inches (4 mils) thick in a stack of paper 4 inches high. In any stack of paper up to this maximum limit, a 10-bit A/D could be used in an electronic system which would sound an alarm if a sheet was added to or removed from the stack. (For simplicity, this assumes we have a perfect height transducer and perfect analog signal conditioning circuitry between this transducer and the input to the A/D.)

If the A/D converter has an accuracy of ± 1 least significant bit (LSB), this could be expressed as $\pm 1/1024$ or $\pm 0.1\%$ of full-scale.

10 BITS PRESENTS DESIGN PROBLEM

An A/D converter which provides every possible analog voltage as a tap on a resistor ladder would require 2^{10}, or 1024 resistors. A ladder expansion technique has been previously developed which has greatly reduced the number of resistors. This technique has been used to provide an 8-bit A/D (the ADC0804 family) which uses a theoretical minimum of only 7 resistors. (In practice, extra resistors are typically used to improve matching by making use of unit resistors.)

This 8-bit A/D design was the starting point for developing this 10-bit converter. A new idea, which is key to the 10-bit design, is a novel way to, in effect, use the previous 8-bit circuit four times to increase the resolution to 10 bits†. This was achieved by adding 2 MSBs to the 8-bit design. We will first review the 8-bit A/D operation as a basis for understanding the new 10-bit design.

THE BASIC 8-BIT DESIGN

The essential part of the ADC0804 8-bit A/D family is a novel, multiple input, voltage comparator. This circuit allows a new feature for a comparator: multiple, differential voltages can be accepted as simultaneous inputs to the comparator, and each differential input can be weighted by scaling the size of the associated input capacitor. The traditional op amp summing circuit, *Figure 1*, is similar, but accepts single-ended voltage inputs, and first converts each input voltage to an input current by making use of a scaled or weighted input resistor. These input currents are then algebraically summed at the "virtual ground" or summing junction (the $(-)$ input of an op amp which has the $(+)$ input grounded). The current surplus (or deficiency) is supplied through the feedback resistor to produce the output voltage.

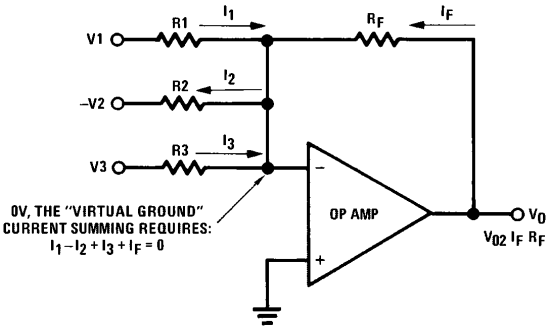

FIGURE 1. The Traditional Op Amp Summing Circuit

†This design concept was proposed and implemented by John Connolly.

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A more useful voltage comparator results from a sampled-data approach, which involves switches and capacitors. Now, input voltages are converted to input charges by the use of input capacitors, and the resulting charges are then algebraically added at a ''charge summing'' node.

A multiple, differential input, sampled-data comparator is shown in *Figure 2* with the switches in the zeroing cycle. The input-output short, which is accomplished with SW5 around the inverting gain block (provided by a logic inverter), causes this stage to bias at a fixed DC voltage. For example, a standard CMOS inverter will bias at approximately one half of the power supply voltage. Notice that at this time the input switches, SW2 and SW4, are precharging the input capacitors with the (−) input voltages of the differential inputs. These input capacitors will serve as storage elements to remember both of the (−) input voltages and the biasing voltage of the gain stage.

These zeroing switches are then opened. The gain stage is now active and will respond to any deviations in the input voltage. An input voltage results when the switches SW1 and SW3 are subsequently both closed. As shown in the figure, ΔV1 is positive, which inputs a charge, Q1, proportional to the value of C1, (Q1 = ΔV1C1). If ΔV2 is negative, a charge, Q2, will be removed from the charge summing node. If the charges Q1 and Q2 are balanced, there is no net change in the input voltage of the inverting gain block.

These switches are dynamically cycled by a clock and the system is zeroed prior to each measuring interval. This is the same operating mode as has been used years ago by the auto-zeroed or chopper-stabilized op amps. A sufficient number of these stages are capacitor-coupled to provide an adequate overall gain for the comparator.

MAKING AN 8-BIT A/D

This sampled-data comparator was made the heart of an 8-bit A/D converter, as shown in *Figure 3*. The comparator now has four differential voltage inputs; one for the analog inputs and three for the DAC. The first 4 MSBs of the 8-bit A/D are supplied by the DAC switches, S1 and S2. As shown, the positions of S1 and S2 correspond to the digital code, ''10 00,'' for the first 4 bits of the 8-bit word. This should input $V_{REF}/2$ from the DAC. Note that S1 is selecting $\frac{3}{4}$ V_{REF} and S2 is selecting $\frac{1}{4}$ V_{REF}, and these voltages are the first differential pair which is sampled by SW1 and SW2 at the start of a successive approximation search. This provides ($\frac{3}{4}$ $V_{REF} - \frac{1}{4}$ V_{REF}) or $\frac{1}{2}$ V_{REF} as required from the DAC.

The differential input feature of this comparator has allowed an unusual resistor ladder to be used for the DAC. Notice that the top three resistors (each labeled ''R'') have $\frac{1}{4}$ V_{REF} across them and the lower resistors (each labeled ''R/4'') have $\frac{1}{16}$ V_{REF} across them. The comparator, therefore, allows the increased resolution of the S2 selected voltages to be ''fitted into'' each section of the upper or S1 selected voltages. In this way, the first 4 bits of this differential DAC, or ''DDAC,'' are realized.

This same 4-bit trick is used again via the left side decoding switches, S3 and S4. These same voltage values provide charge which is reduced in significance by 16:1, making the input capacitor for this section a factor of 16 smaller. This now provides the least significant 4-bit group. The additional capacitor, C, and the lowermost two resistors (labeled ''R/8'') supply a $\frac{1}{2}$ LSB overall DAC offset voltage. This is used in A/Ds to center the natural $\pm\frac{1}{2}$ LSB quantization uncertainty of the A/D about the integer LSB values of analog input voltage. (This is $\frac{1}{2}$ LSB voltage is added to the analog input to cause the 00_{HEX} to 01_{HEX} code change of the A/D to occur at any analog input voltage value of only $\frac{1}{2}$ LSB.)

If we are to use this basic 8-bit design for a 10-bit converter, we must make these 8 bits the least significant of the 10-bit data word. This can easily be done by again scaling the capacitor sizes. Further, 2 additional MSBs must be added: here is where another trick comes in.

A NOVEL WAY OF ADDING 2 MSBs

The 2 MSBs of the DAC will control 2^2, or 4, voltages. If these are chosen as V_{REF}, ground, $\frac{1}{3}$ V_{REF} and $\frac{2}{3}$ V_{REF} we have an unusually beneficial situation. Notice that the differential voltage input feature of the sampled-data comparator allows picking up the two intermediate voltages ($\frac{1}{3}$ and $\frac{2}{3}$ V_{REF}) from a resistor divider with only one tap, as shown in *Figure 4*. These odd voltage values ($\frac{1}{3}$ and $\frac{2}{3}$ V_{REF}) from this 2 MSB DAC are ''cleaned up'' simply by scaling the size of the input capacitor which is used for this DAC section by a factor of $\frac{3}{4}$. This will, therefore, provide the $\frac{1}{4}$ V_{REF} increments 0, $\frac{1}{4}$ V_{REF}, $\frac{2}{4}$ V_{REF} and $\frac{3}{4}$ V_{REF}, which are necessary for the 2 MSBs. Now the basic 8-bit circuit can be used a total of 4 times, with each referenced to one of these $\frac{1}{4}$ V_{REF} values. This will cover the analog input voltage range of 0 to V_{REF} with 10 bits of resolution, as shown in *Figure 5*.

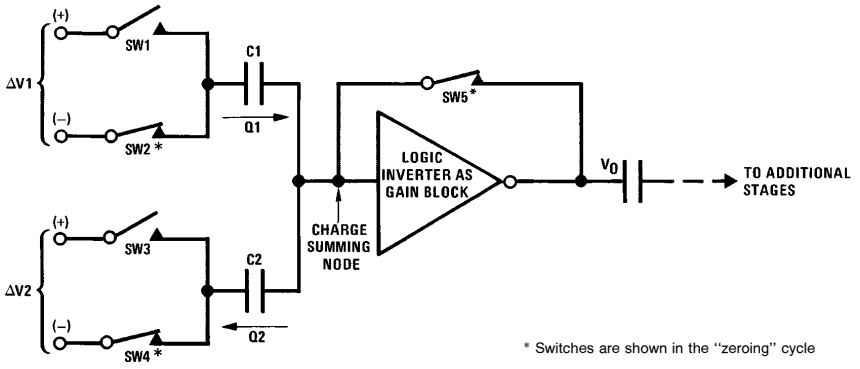

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FIGURE 2. A Multiple, Differential Input Sampled-Data Comparator or Charge Summing Circuit

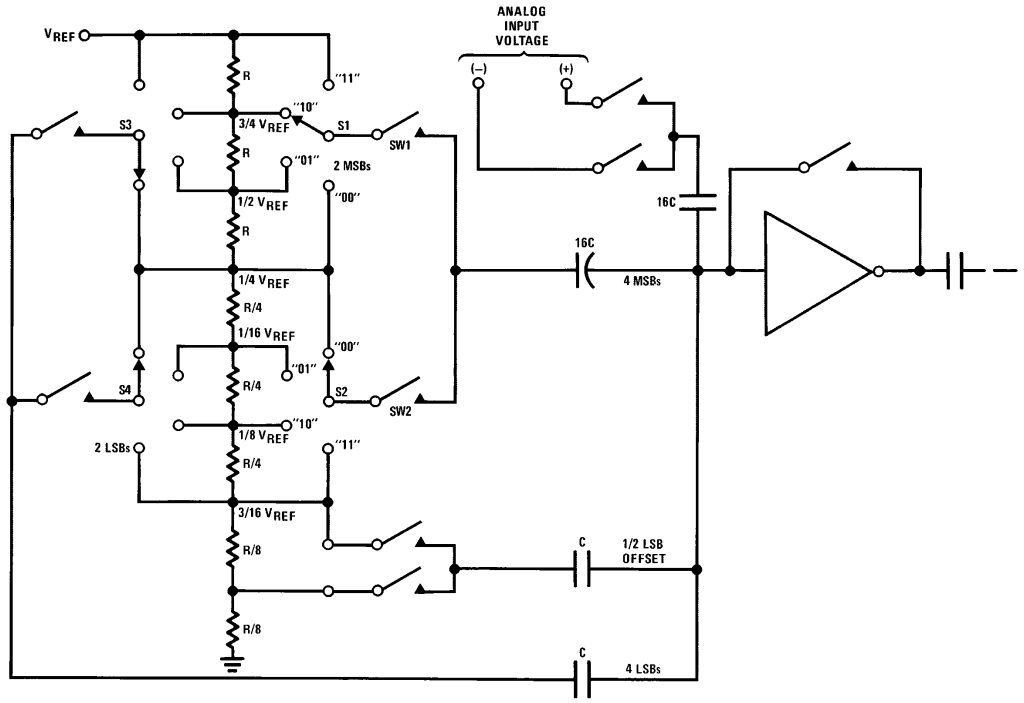

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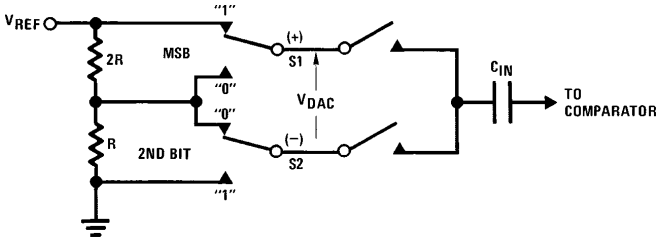
FIGURE 3. Basic DAC Ladder of 8-Bit A/D Converter



S1 (MSB)	S2 (2nd Bit)	V_{DAC}
0	0	0
0	1	$\frac{1}{3} V_{REF}$
1	0	$\frac{2}{3} V_{REF}$
1	1	V_{REF}

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FIGURE 4. Providing the 2 MSBs of a 10-Bit A/D

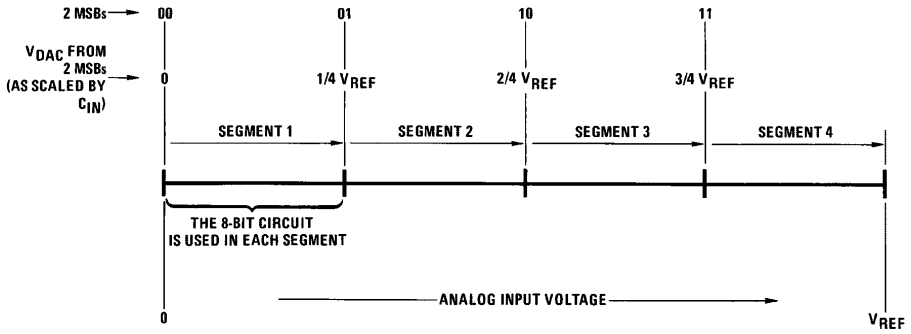

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FIGURE 5. How the 2 MSBs Extend the 8-Bit Circuit to 10 Bits

This 2 resistor ladder will produce linearity errors in only 2 of the segments of the overall A/D transfer characteristic, because there will be no errors in the first segment (2 MSBs = 0), because V_{DAC} for this code is 0V. Similarly, if we assume that the input capacitors ratio properly, there will be no linearity errors in the last segment, because the full V_{REF} is sampled (then is weighed to produce ¾ V_{REF} as compared to the analog input voltage, via C_{IN}). Any mismatch between the C_{IN} of the analog differential input voltage and the C_{IN} of the DACs will cause a full-scale error, not a linearity error.

The two end segments are therefore both free of linearity errors and an additional benefit is that any error in the exact value of the tap voltage on a 2 resistor divider has the natural characteristic that the error is the same magnitude on the ⅓ V_{REF} and ⅔ V_{REF} voltages, and is simply of opposite sign. Thus, a linearity trim must provide a single magnitude of correcting charge, then this same charge is introduced into the comparator summing mode in one polarity for the "01" 2 MSB code, and then the opposite polarity for the "10" code (a correcting charge is not used for the "00" or "11" codes).

THE ADC1001, A 10-BIT A/D

In keeping with the similarity to the previous 8-bit A/D, a 10-bit product was designed to fit in the same 20 pin (0.3″ wide) package and to use the same pinouts. Now a customer can easily interchange from an 8 to a 10-bit A/D. This allows for a range of performance variation in his end products while using the same PC board.

The problem of getting the 10-bit output of the A/D onto an 8-bit data bus is handled by reading two 8-bit bytes. The data is left-justified and transferred, most significant byte first. This allows a single read cycle to pick up a valid 8-bit representation (the 8 MSBs) and can save time if this is all the resolution that is required on a particular analog channel. A second read cycle will pick up the 2 LSBs of the 10-bit data word. The 6 LSB positions are set to zero in this second byte. An internal byte counter keeps track of the byte sequencing so multiple, double-read cycles can be made, if desired.

The problem of properly biasing a 5 V_{DC} reference circuit when operating from only a single 5 V_{DC} power supply voltage was handled on the 8-bit part by reducing the operating reference voltage for the internal DAC to only 2.5 V_{DC}. This can be designed to still provide a 5V full-scale for the A/D by simply doubling the sizes of all of the DAC input capacitors to the comparator. This technique was also used for this 10-bit product. The reference voltage can also be further reduced in magnitude to increase the analog resolution over a reduced analog input voltage span, if desired.

A basic diagram of the DAC and the comparator input section of the 10-bit A/D are shown in *Figure 6*. A simplified schematic representation has been used for the 8 LSB section. This has been shown in more detail in *Figure 3* without the V_{REF} reduction to $V_{REF}/2$.

To understand the scaling shown for the input capacitors, keep in mind that it is the input charge which is balanced. This means that a maximum differential analog input voltage of 5V would produce an input charge of 5 x 32C or 160C

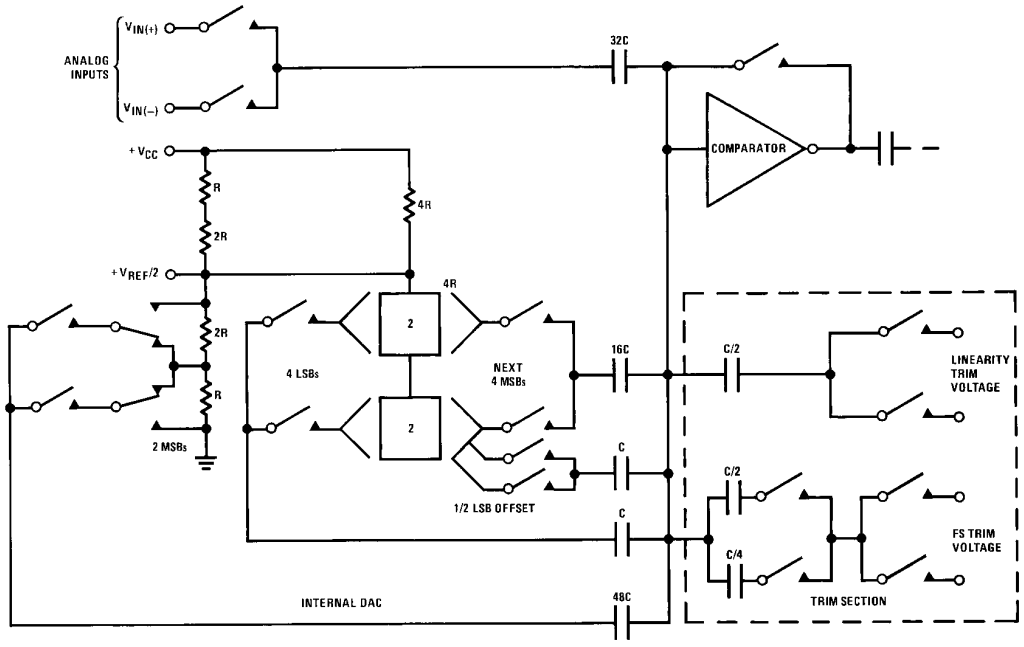

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FIGURE 6. The DAC and Comparator Input Section

coulombs. If the DAC were forced to a ''11 0000 0000'' or 300_{HEX} code, the voltage, which is output from the 2 MSB section, would be $V_{REF}/2$. This is converted to an input charge via the 48C capacitor, so this charge, $Q300_{HEX}$, becomes:

$$Q300_{HEX} = \frac{V_{REF}}{2} \times 48C$$

and as $V_{REF}/2 = 2.5V$

then

$$Q300_{HEX} = 2.5\,(48)C$$

or

$$Q300_{HEX} = 120C$$

which ratios to the analog full-scale charge, Q_{AFS} as

$$\frac{Q300_{HEX}}{Q_{AFS}} = \frac{120C}{160C} = \frac{3}{4}\,FS$$

which is the proper weight for the 300_{HEX} code.

Similarly, the ''00 1000 0000'' or 080_{HEX} code should require $\frac{1}{8}$ (V_{REF}) at the analog input (neglecting the effects of the $\frac{1}{2}$ LSB offset voltage shift) to balance. This is the output of the 8 LSB section with a binary code of ''1000 0000'' input to this DAC section. The charge from the analog input, Q_A, which corresponds to an analog input voltage of $\frac{1}{8}$ V_{REF}, is given by:

$$Q_A = \tfrac{1}{8}(V_{REF})\,(32C)$$

The output voltage of the 8-bit DAC section for 080_{HEX} code is $\frac{1}{2}$ (V_{REF})/2, so the charge input by this DAC, Q_{DAC}, is given by

$$Q_{DAC} = \tfrac{1}{2}\frac{(V_{REF})}{2}\,(16C),$$

and this ratios to the analog input change, Q_{A1}, as

$$\frac{Q_{DAC}}{Q_A} = \frac{\frac{1}{2}\,(V_{REF}/2)\,(16C)}{\frac{1}{8}\,(V_{REF})\,(32C)} = 1$$

as expected. The 4 LSB grouping of this 8-bit DAC uses an input capacitor $\frac{1}{16}$ smaller in value to properly reduce the significance of the last 4 bits.

FULL-SCALE TRIM

Full-scale (or ''gain'') errors are trimmed by introducing an additional correcting charge into the summing node of the comparator. This is done in steps; for example, no full-scale correction is used on the first $\frac{1}{4}$ of the analog input voltage range (near zero). The next range receives $\frac{1}{3}$ of the total FS correcting charge, then $\frac{2}{3}$, and finally the full charge is introduced in the last section. This sequencing of the FS trim is achieved by dynamically altering the input capacitance from no capacitance to C/2, to C/4, and finally to 3C/4. This is the reason for the extra input capacitor and the added switches, which are shown in the FS trim section of *Figure 6*.

APPLICATIONS

The standard applications of the 8-bit ADC0804 series* can now easily be extended to 10 bits by simply plugging in the new ADC1001 10-bit part. In addition, a 24 pin product (ADC1021) is also available, which brings all 10 bits out for a 16-bit data bus application.

The zero offsetting (by introducing a DC shifting voltage into the $V_{IN(-)}$ pin) can be used to accommodate analog input voltages which do not swing to ground. The $V_{REF}/2$ input voltage can also be reduced to accommodate a reduced span of analog input voltages. Finally, system designers can use the same PC board for either an 8-bit or a 10-bit product to take advantage of the standard pinouts used for these A/D converters.

CONCLUSIONS

The multiple, input, sampled-data voltage comparator allows many benefits in both the design and application flexibility of monolithic A/D converters. This revolutionary concept has reduced the die size of A/Ds, allows many product benefits, and appears to be the optimum solution for the realization of a low cost, high performance, monolithic A/D converter line.

*For further details see data sheet.

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